A VOLTAGE CONTROLLED OSCILLATOR DELAY CELL

Field of the Invention

[0001] The present invention relates to oscillators in general, and, more particularly, to voltage-controlled ring oscillators.

Background of the Invention

[0002] The voltage-controlled oscillator (VCO) is an important building block in phase-locked loops, clock recovery circuits, and frequency synthesizers. High frequency and radio frequency (RF) voltage-controlled oscillators can be implemented monolithically as LC oscillators, as relaxation oscillators and ring oscillators. Ring oscillators are frequently used in the prior art to generate high frequency clock signals. Ring oscillators may be controlled by a voltage or current source to generate a variable frequency signal.

[0003] Figure 1 depicts a block diagram of delay cells arranged as a ring voltage-controlled oscillator of the prior art. Ring oscillator 100 comprises multiple stages of amplification and delay that are connected in tandem, with the last stage coupled back to the first stage in the form of a ring around which the signals propagate. Each stage of the ring oscillator, labeled 100-1 through 100-3 in the figure, provides a phase shift. In particular, each half period the signal will propagate around the delay cell ring with an inversion. Ring oscillators can be implemented using differential pair or current-starved single-ended inverter structures.

[0004] Figure 2 depicts a schematic of a typical differential amplifier with resistive loads to implement a single delay cell. Parasitic capacitances across the drain-to-source of transistors M1 and M2 interact at high frequency with resistors R1 and R2 to provide the requisite phase shift and gain of the delay cell. Figure 3 is a variation of figure 2 in which the resistors have been replaced by MOS transistors M4 and M5. The resistors of figure 1 occupy a large area on a die, which can be alleviated in figure 2 by transistors, covering a smaller area, the latter operating in their ohmic regions to act as resistive loads. It has been recognized in the prior art that it is beneficial to use differential amplifiers for each of the stages of the ring oscillator in order to cause the oscillator to be more immune to the influence of spurious noises in the form of voltage and current spikes that might be coupled to both sides of the differential circuit. Such a spurious noise from the power supply, for example, would be coupled to both sides of the differential amplifier, and it would therefore

affect both of the sides of the differential stages substantially equally. Consequently, the effect of such spurious noise is minimized on the output of the oscillator, which can be taken as the difference of the outputs of any one of the stages.

[0005] Two problems associated with using differential amplifiers in a ring oscillators are differential mode lockup and common mode lockup. Differential mode lockup refers to the phenomenon that occurs where each stage (differential amplifier) of the ring oscillator would end up with its output at either the opposite voltage limits or at the same voltage limit as the other stages. However, differential mode lockup typically only occurs in a ring oscillator with an even number of stages (*e.g.*, 2, 4, 6, *etc.*). For example, in a simple two stage ring oscillator, differential lockup could occur with the first output of stage one and the second output of stage two sitting at one voltage limit while the second output of stage one and the first output of stage two are sitting at the opposite voltage limit. Common mode lockup could occur with the first and second outputs of stage one sitting near one voltage limit while the first and second outputs of stage two are sitting near the opposite voltage limit.

[0006] Differential mode lockup can be prevented in a ring oscillator using an even number of stages by crossing the connections made between the outputs and the inputs for one pair (or an odd number of pairs) of connections in the ring oscillator. As a result, an additional phase inversion is provided in the differential signal path, and lockup of the oscillator on a differential basis is prevented. Alternatively, figure 4 depicts the resistive loads replaced by monolithic inductors. The inductors, along with the parasitic capacitors of the transistors M1 and M2, form an LC oscillator, which is free of the latch up problems of the resistive load delay cell. This configuration suffers from being dependent on large physical inductors that are hard to match and, together with the parasitic capacitance, hard to tune the oscillation frequency.

[0007] The oscillation frequency of LC topologies is equal to

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$ suggesting that only the inductor and capacitor values can be varied to tune the frequency. Since it is difficult to vary the values of the monolithic inductors and the parasitic capacitances, we can replace the parasitic capacitance with a voltage dependent capacitor called a "varactor." Figure 5 shows diodes D1 and D2 as reversed biased PN junctions acting as varactors added as shown to the circuit of Figure 4. VC sets the voltage

across diodes D1 and D2, producing a tuning range for the capacitance values which in turn tunes the LC oscillator.

[0008] Besides the above-mentioned limitation of monolithic inductor implementations, the PN junction-type varactor has a very limited range of reverse bias voltage, yielding a limited range of tuning frequency.

Summary of the Invention

[0009] To provide greater tuning range than that provided by "varactor" diodes, the diodes are replaced with PMOS transistors in series with the drains of transistors M1 and M2 of figure 5. The drain and sources of the PMOS transistors are electrically connected to each other, so that voltage-dependant CMOS capacitors are formed between the gate-to-source terminals and the gate-to-drain terminals of the PMOS transistor.

[0010] Secondly, the monolithic inductors of Figure 5 are replaced by "active" inductors: the combination of a resistor connected in series with the gate of an NMOS transistor, where the potential at the drain of the NMOS transistor is held below that of the second terminal of the resistor by at least the threshold, or turn-on voltage, of the transistor, acts inductively at the frequency of oscillation of interest. The differential amplifier structure is maintained from Figure 5.

[0011] The illustrative embodiment comprises: a first NMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal; a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first NMOS field effect transistor; a first PMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal, wherein said source terminal of said first PMOS field effect transistor is electrically connected to said source terminal of said first NMOS field effect transistor; and a second NMOS field effect transistor having a gate terminal, a source terminal, and a drain terminal, wherein said drain terminal of said second NMOS field effect transistor is electrically connected to said drain terminal of said first PMOS field effect transistor, and wherein said drain terminal of said first PMOS field effect transistor is electrically connected to said source terminal of said first PMOS field effect transistor.

Brief Description f the Drawings

[0012] Figure 1 depicts a block diagram of delay cells arranged as a ring voltage-controlled oscillator of the prior art.

[0013] Figure 2 depicts a schematic of a typical differential amplifier with resistive loads to implement a single delay cell.

[0014] Figure 3 is a variation of figure 2 in which the resistors have been replaced by MOS transistors M4 and M5.

[0015] Figure 4 depicts the resistive loads replaced by monolithic inductors.

[0016] Figure 5 shows diodes D1 and D2 as reversed biased PN junctions acting as varactors added as shown to the circuit of Figure 4.

[0017] Figure 6 depicts a schematic diagram of the salient components of the illustrative embodiment of the present invention.

[0018] Figure 7 depicts a schematic of the small signal model for the active inductor of Figure 6.

[0019] Figure 8 depicts a bode-plot of the magnitude of Z_o as a function of frequency.

[0020] Figure 9 depicts a schematic of the small signal model for the CMOS capacitor constructed from an MOS transistor.

Detailed Description

[0021] Figure 6 depicts a schematic diagram of the salient components of the illustrative embodiment of the present invention. Resistor R1 is connected at one end to a positive power supply V_{DD2} at 601, and at its other end to the gate terminal of NMOS transistor M6. The drain terminal of NMOS transistor M6 is connected to a second power supply rail V_{DD1} at 602. For the preferred embodiment, this supply voltage is about 1.8 volts. V_{DD2} must be greater than V_{DD1} by at least the threshold voltage of transistor M6 for the active inductor formed by R1 and M6 to operate, *i.e.*, the transistor M6 must operate in its active region. The combination of R1 and M6 is called active inductor AI_1, to be described in figure 7.

[0022] The source of transistor M6 is connected to the source of PMOS transistor M4, labeled V_{OUT}^-, while the drain terminal of transistor M4 is connected to the drain terminal of NMOS transistor M1 at 603-1. The source of transistor M4 is connected to the drain of transistor M4. Transistor M4 with drain to source terminals shorted is called CMOS capacitor CC_1, to be described further in figure 8. The source terminal of transistor M1 is connected to

the drain terminal of NMOS transistor M3, while the source terminal of transistor M3 is electrically connected to ground potential.

[0023] The remaining transistors and resistor are the mirror images of those already described so as to form a differential pair. The drain of transistor M3 is connected to the source of NMOS transistor M2. The drain of PMOS transistor M5 is connected to the drain of transistor M2 at 603-2, while the gate of transistor M5 is connected to the gate of transistor M4. The source of transistor M5 is connected to the source of NMOS transistor M7, labeled V_{OUT}^+. The drain of transistor M5 is connected to the source of transistor M5. Transistor M5 with drain to source shorted is called CMOS capacitor CC_2, to be described in figure 8. The drain of transistor M7 is connected to power supply V_{DD1} at 602. The gate of transistor M7 is connected to one end of resistor R2, while the other end of transistor R2 is connected to supply voltage V_{DD2} at 601. The combination of R2 and M7 is called active inductor AI_2, to be described in figure 7.

[0024] The gate of transistor M1 is labeled as differential positive input voltage V_{in}^+, while the gate of transistor M2 is labeled as differential negative input voltage V_{in}^-. A differential input voltage from a previous delay cell stage is connected to these inputs. The gate terminals of both transistor M4 and M5 are labeled as control voltage $V_{control}$, which is the voltage control terminal that varies the LC oscillator circuit capacitance. The source of transistor M6 is labeled as differential negative output voltage V_{out}^-, while the source of transistor M7 is labeled as differential positive output voltage V_{out}^+. The differential output leads are connected to the differential inputs of another delay cell. A bias voltage, labeled V_{bias}, is connected to the gate of transistor M3 to provide a constant DC bias current to the differential pair circuit. The circuit as a whole is differential input/output to as to reduce the circuit's susceptibility to noise.

[0025] In the prior art of figure 5, the LC portion of the differential pair oscillator cell was realized by a physical passive inductance component, and a varactor diode that was reverse biased to provide the variable capacitor function. This variable capacitor, which sets the oscillation frequency, is controlled by a voltage applied to the cathode of the diode.

[0026] In Figure 6, the passive inductor is replaced by what is called an active inductor. There are two active inductors in the illustrative embodiment: one comprising resistor R1 and NMOS transistor M6, and a second comprising resistor R2 and NMOS transistor M7.

[0027] Figure 7 depicts schematics of the small signal model for the active inductors of Figure 6. Figure 7a represents active inductor AI_1 of figure 6, while figure 7b represents

active inductor AI_2 of figure 6. The DC power supply rails at 601 and 602 have been replaced by AC ground potentials. For the analysis we will look at figure 7a. At node V_g, we have

$$sC_{gs1}(V_g - V_{o1}) + \frac{V_g}{R1} + V_g sC_{gd1} = 0 \tag{Eq. 1}$$

Rearranging slightly, we have

$$V_g = \frac{sC_{gs1}R1V_{o1}}{1 + sR1(C_{gs1} + C_{gd1})} \tag{Eq. 2}$$

At node V_{OUT}^-,

$$I_{o1} = g_{m1}(V_g - V_{o1}) + (V_g - V_{o1})sC_{gs1} - V_{o1}sC_L \tag{Eq. 3}$$

Solving (2) and (3), we have

$$Z_o = \frac{V_{o1}}{I_o} = \left[\frac{1 + sR1(C_{gs1} + C_{gd1})}{[R1(C_{gd1}C_{gs1} + C_{gs1}C_L + C_{gd1}C_L)]s^2 + [(C_{gs1} + C_L + g_{m1}R1C_{gd1})]s + g_{m1}} \right] \tag{Eq. 4}$$

From equation (4) the poles (6 and 7) and zero (5) can be identified as:

$$Z_1 = \frac{1}{R1(C_{gs1} + C_{gd})} \tag{Eq. 5}$$

$$P_1 = \frac{g_{m1}}{C_{gs1} + C_L + g_{m1}R1C_{gd1}} \tag{Eq. 6}$$

$$P_2 = \frac{C_{gs1} + C_L + C_{gd1}}{R1(C_{gs1}C_{gd1} + C_LC_{gd1} + C_LC_{gs1})} \tag{Eq. 7}$$

Figure 8 depicts a bode-plot of the magnitude of Z_o as a function of frequency. In the range of frequency between Z_1 and P_1, the active inductor induces a zero, increasing gain with frequency, similar in function to a real inductor. The active inductor introduces inductive impedance as a load at the oscillator frequencies of interest.

The varactor diodes are replaced by two PMOS transistors, M4 and M5, respectively. For each transistor, the source terminal is electrically connected to the drain terminals. A variable capacitor is formed by the PN junction comprising the semiconductors between the drain and gate terminal of M6, or between the drain and gate terminal of M7. In this CMOS

capacitor, the gate acts as a plate and the drain and source connected together act as a second plate. The two plates are separated by silicon oxide, which acts as a dielectric, and this configuration makes the MOS transistor act as a capacitor.

The varactor effect is achieve by applying a positive voltage to the gate terminal of M4 in the range of 0.9 to 1.3 Volts for the case of a supply voltage of 1.8 volts with 0.18 micron CMOS technology. It will be clear to those skilled in the art, however, how to make and use alternative embodiments of the present invention in which the supply voltage and process technology can be varied to give different ranges of control voltage and hence different tuning ranges of the LC oscillator.

Figure 9 depicts a schematic of the small signal model for the CMOS capacitor constructed from an MOS transistor. Figure 8a depicts the high frequency model of the MOS transistor from the perspective of CC_1 of Figure 6, with the addition of the drain terminal being electrically connected to the source terminal. Figure 8b depicts the small signal model of CMOS capacitor CC_2 of Figure 6. The analysis for both CMOS capacitors is the same.

Terminal B, which is electrically connected to AC ground, is the bulk or substrate connection of the device not normally shown in transistor schematics. When the drain terminal is electrically connected to the source terminal, the dependent sources, $g_m V_{gs}$ and $g_{mb} V_{bs}$, are shorted, as well as the output resistance r_o. The schematics of figures 8a and 8b reduce to that of figure 8c, which shows a gate to bulk capacitance, C_{gb}, a drain to bulk capacitance, C_{db} in parallel with source to bulk capacitance , C_{sb}, and gate to drain/source capacitances C_{gd} and C_{gs} in parallel. Since C_{gb} and C_{db} are negligible compared to C_{sb} and the combination of C_{gd} and G_{gs}, C_{gb} and C_{db} can be ignored. The circuit further reduces to figure 8d. The relationship between the gate control voltage and the device capacitance is as follows: Taking node V_g as a reference, we have

$$\frac{V_g - V_d}{(C_{gd} + C_{gs})s} = \frac{V_d}{sC_{sb}} \qquad \text{(Eq. 8)}$$

and

$$V_g - V_d = V_{gd} \qquad \text{(Eq. 9)}$$

Rearranging (8) gives

$$V_{gd} = \frac{V_d}{C_{sb}}(C_{gd} + C_{gs}) \qquad \text{(Eq. 10)}$$

The voltage at the gate is proportional to the gate-drain and gate-source capacitances.

[0028] It is to be understood that the above-described embodiments are merely illustrative of the present invention and that many variations of the above-described embodiments can be devised by those skilled in the art without departing from the scope of the invention. It is therefore intended that such variations be included within the scope of the following claims and their equivalents.

[0029] What is claimed is: